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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,602	BRINK ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 24th of April 2006. Claims 1, 3, 4, 6, 9, 13-17, 19-22, and 24-27 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 24th of January 2006. Currently, claims 1-27 are pending in this Application.

Claim Objections

2. Claims 13, 21, and 25 are objected to because of the following informalities:

The claims 13 and 21 recite the subject matter "the memory device" in line 5 of the claim 13, and in lines 5-6 of the claim 21, respectively. However, it has not been specifically clarified in the respective claims 13 and 21. Therefore, the Examiner presumes that the term "the memory device" could be considered as --a memory device-- in light of the specification since it is not defined in the claims.

The claim 25 recites the subject matter "the second processor" in line 3. However, it has not been specifically clarified in the claim 25 and its intervening claims. Therefore, the Examiner presumes that the term "the second processor" could be considered as --a second processor-- in light of the specification since it is not defined in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh [US 5,935,233 A] in view of Athenes et al. [US 6,192,441 B1; hereinafter Athenes] and Moyer et al. [US 6,976,110 B2; hereinafter Moyer].

Referring to claim 1, Jeddeloh discloses an integrated circuit (i.e., PCI host bridge 56 of Fig. 2) comprising:

- a peripheral interface (i.e., first PCI interface 86 of Fig. 2);
- a memory interface (i.e., memory interface 84 of Fig. 2) to communicate with a memory device (i.e., system memory 58 of Fig. 2; See col. 3, lines 54-56);
- a processor interface (i.e., processor interface 82 of Fig. 2) to communicate with a processor (i.e., processor 52 of Fig. 2; See col. 3, lines 51-53); and
- a logic circuit (i.e., control switch 90 of Fig. 2) connected to the peripheral interface (i.e., said first PCI interface is connected to said Control switch in Fig. 2), wherein
    - the logic circuit (i.e., said control switch) is also connected to the processor interface and the memory interface (i.e., said first PCI interface and said processor interface are connected to said control switch in Fig. 2).

Jeddeloh does not teach that the peripheral interface receives an interrupt request; and the logic circuit acquires an interrupt information associated with the interrupt request, wherein the logic circuit is to pass the interrupt information to the memory device without passing the interrupt information to the processor interface; and a configuration circuit configured to store configuration address indicating a location in the memory device to store the interrupt information.

Athenes discloses an apparatus for postponing processing of interrupts by a microprocessor (See Abstract), wherein

- a peripheral interface (i.e., 16-bits buses between entities U1-U3 and interrupt control device 3 in Fig. 1) receives an interrupt request (i.e., event justifying an interruption; See col. 3, lines 19-22);
- a logic circuit (i.e., interrupt control device 3 of Fig. 1) acquires an interrupt information (i.e., the origin of interrupt and reason for the interruption event) associated with the interrupt request (See col. 3, lines 21-22 and col. 4, lines 38-44), wherein
    - the logic circuit (i.e., said interrupt control device) is to pass the interrupt information to a memory device (i.e., RAM 2 of Fig. 1) without passing the interrupt information to a processor interface (See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller implies that the logic circuit passes the interrupt information to a memory device without passing the interrupt information to a processor interface); and
- a configuration circuit (i.e., logic circuit 4 and registers 6,7 in Fig. 1) configured to store configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3,

lines 30-35 and col. 4, lines 45-52) indicating a location in the memory device (i.e., RAM 2 of Fig. 1) to store the interrupt information (See col. 4, lines 53-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said integrated circuit (i.e., interrupt control device), as disclosed by Athenes, in said logic circuit (i.e., control switch), as disclosed by Jeddeloh, for the advantage of avoiding a risk of operation error that a subsequent interrupt signal (i.e., event) interrupts the processing of a preceding interrupt of the same type, issued by a same entity (See Athenes, col. 2, line 67 through col. 3, line 3).

Jeddeloh, as modified by Athenes, does not teach that the configuration circuit is further configured to store configuration data indicating a number of devices the integrated circuit is configured to handle.

Moyer discloses an apparatus for reducing interrupt latency by dynamic buffer sizing (See Abstract), wherein

- a configuration circuit (i.e., Store Buffer of Fig. 1) is configured to store configuration data (i.e., limit control register 141 storing limit value of ADA slots in Fig. 2) indicating a number of devices* (i.e., a number of ADA slots in Fig. 2) an integrated circuit (i.e., Processor 102 of Fig. 1) is configured to handle (See col. 4, lines 4+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., Store Buffer), as disclosed by Moyer, in said integrated circuit (i.e., PCI host bridge), as disclosed by Jeddeloh, as modified by Athenes, for the advantage of providing the ability to decouple writes to long latency memory with reducing interrupt latency by dynamic buffer sizing (See Moyer, col. 1, lines 21-28 and col. 3, lines 6-32).

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* "device"$_n$ is defined as "a mechanism designed to serve a special purpose" by Merriam-Webster's Collegiate® Dictionary (10th ed.)

Referring to claim 2, Athenes teaches

- a memory unit (i.e., FIFOs 8-10 in Fig. 1) to store the interrupt information (i.e., the origin of interrupt and reason for the interruption event) before the interrupt information is passed to the memory interface (i.e., n-bits bus 5 between logic circuit 4 and RAM 2 in Fig. 1; See col. 5, lines 32-48).

Referring to claim 5, Jeddeloh teaches

- a graphics interface (i.e., second PCI interface 88 of Fig. 2) to communicate with a graphics card (i.e., graphics controller 74 of Fig. 2; See col. 3, lines 40-44 and 62-67).

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh [US 5,935,233 A] in view of Athenes [US 6,192,441 B1] and Moyer [US 6,976,110 B2] as applied to claims 1, 2, and 5 above, and further in view of Tseng et al. [US 6,816,918 B2; hereinafter Tseng].

Referring to claim 3, Jeddeloh, as modified by Athenes and Moyer, discloses all the limitations of the claim 3, except that does not expressly teach the configuration circuit including a read only memory to store the configuration data.

Tseng discloses a flexible apparatus for setting configurations using an EEPROM (See Abstract), wherein

- a configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM in Fig. 3) including a read only memory device (i.e., said EEPROM in Fig. 3) to store configuration data (i.e., storing address index and its contents; See col. 3, lines 35-39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM), as disclosed by Tseng, in said configuration circuit (i.e., logic circuit and registers), as disclosed by Jeddeloh, for the advantage of providing a method for flexibly configuring default location in the memory device (i.e., default value) of the integrated circuit (i.e., network device) through the read only memory (i.e., EEPROM interface; See Tseng, col. 2, lines 28-30).

Referring to claim 4, Tseng teaches

- the read only memory device (i.e., EEPROM in Fig. 3) is to store the configuration address (i.e., storing address index and its contents; See col. 3, lines 35-39).

7. Claims 6-8, 10, 11, 21, 22, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson et al. [US 6,466,226 B1; hereinafter Watson] in view of Athenes [US 6,192,441 B1] and Moyer [US 6,976,110 B2].

Referring to claim 6, Watson discloses a system (i.e., computer system in Fig. 2) comprising:

- a processor (i.e., one of the one or more processors 110 in Fig. 2; See col. 3, lines 60-64);
- a memory device (i.e., system memory 130 of Fig. 2); and
- a chipset (i.e., chipset 200 of Fig. 2) connected to the processor and the memory device (i.e., said processor and said system memory are connected to said chipset in Fig. 2; See col. 5, lines 19-32).

Watson does not expressly teach that the chip set is configured to receive interrupt information and to pass the interrupt information to the memory device without notifying the processor the presence of the interrupt information; and the chipset includes an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in the memory device to store the interrupt information.

Athenes discloses an apparatus for postponing processing of interrupts by a microprocessor (See Abstract), wherein

- a chipset (i.e., System control components in Fig. 1) to receive interrupt information (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44) and to pass the interrupt information to a memory device (i.e., RAM 2 of Fig. 1) without notifying a processor the presence of the interrupt information (See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller implies that the chipset is configured to pass the interrupt information to a memory device without notifying a processor the presence of the interrupt information); and
- the chipset (i.e., said System control components) includes an interrupt controller (i.e., interrupt control device 3 of Fig. 1) having a configuration circuit (i.e., logic circuit 4 and registers 6,7 in Fig. 1),
    - wherein the configuration circuit (i.e., said logic circuit and registers) is configured to store configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-52) indicating a location in the

memory device (i.e., RAM 2 of Fig. 1) to store the interrupt information (See col. 4, lines 53-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said chipset (i.e., System control components), as disclosed by Athenes, in said chipset, as disclosed by Watson, for the advantage of avoiding a risk of operation error that a subsequent interrupt signal (i.e., event) interrupts the processing of a preceding interrupt of the same type, issued by a same entity (See Athenes, col. 2, line 67 through col. 3, line 3).

Watson, as modified by Athenes, does not teach that the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle.

Moyer discloses an apparatus for reducing interrupt latency by dynamic buffer sizing (See Abstract), wherein

- a configuration circuit (i.e., Store Buffer of Fig. 1) is configured to store configuration data (i.e., limit control register 141 storing limit value of ADA slots in Fig. 2) indicating a number of devices (i.e., a number of ADA slots in Fig. 2) an interrupt controller (i.e., Control Logic 142 of Fig. 2) is configured to handle (See col. 4, lines 4+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., Store Buffer), as disclosed by Moyer, in said integrated circuit (i.e., PCI host bridge), as disclosed by Watson, as modified by Athenes, for the advantage of providing the ability to decouple writes to long latency memory with reducing interrupt latency by dynamic buffer sizing (See Moyer, col. 1, lines 21-28 and col. 3, lines 6-32).

Referring to claim 7, Watson teaches

- the chipset (i.e., chipset 200 of Fig. 2) includes a graphic and memory control hub (i.e., GMCH 210 of Fig. 2) to process graphic and memory information (See col. 5,lines 19-23) and to provide access between the processor (i.e., said one of the one or more processors 110 in Fig. 2) and the memory device (i.e., system memory 130 of Fig. 2; See col. 5,lines 23-32).

Referring to claim 8, Watson teaches

- the chipset (i.e., chipset 200 of Fig. 2) includes an input output control hub (i.e., ICH 220 of Fig. 2) connected to the graphic and memory control hub (i.e., GMCH 210 of Fig. 2; See col. 5, lines 28-32) to process input output information between the chipset and external devices (e.g., display 150, USB devices, and AC'97 devices, etc. in Fig. 2; See col. 5, line 32 through col. 6, line 12).

Referring to claim 10, Watson, as modified by Athenes and Moyer, teaches

- the processor (i.e., said one of the one or more processors 110 in Fig. 2 in Watson, which is mapped to microprocessor 1 of Fig. 1 in Athenes) is configured to poll the memory device (i.e., RAM 2 of Fig. 1; Athenes) to check for the interrupt information (See Athenes, col. 5, lines 61-63) at a time independent from a time the interrupt information is received by the chipset (See Athenes, col. 2, lines 59-67).

Referring to claim 11, Watson teaches

- a second processor (i.e., the other one of the one or more processors 110 in Fig. 2; See Watson, col. 3, lines 60-64) connected to the chipset (i.e., chipset 200 of Fig. 2).

Referring to claim 21, Watson discloses a method (i.e., method for pixel filtering in a computer system; See Abstract) comprising:

- receiving signal at a chipset (i.e., chipset 200 of Fig. 2), the chipset connecting to a first processor (i.e., one of the one or more processors 110 in Fig. 2; See col. 3, lines 60-64) and the memory device (i.e., said processor and said system memory are connected to said chipset in Fig. 2; See col. 5, lines 19-32).

Watson does not expressly teach that receiving an interrupt request at the chipset; acquiring, at the chipset, interrupt information corresponding to the interrupt request, wherein the chipset includes and an interrupt controller having a configuration circuit, wherein the configuration circuit is configured to store configuration address indicating a location in a memory device to store the interrupt information; storing the interrupt information at a memory location without notifying the first processor the interrupt request; and polling the memory device to check for the interrupt information, wherein polling is performed at a time independent from a time the interrupt request is received at the chipset.

Athenes discloses a method (i.e., method of postponing processing of interrupts by a microprocessor; See Abstract) comprising:

- receiving an interrupt request (i.e., event justifying an interruption) at a chipset[†] (i.e., System control components in Fig. 1), the chipset (i.e., said System control components) connecting to a first processor (i.e., microprocessor 1 of Fig. 1; See col. 3, lines 9-22);
- acquiring, at the chipset (i.e., at said System control components), interrupt information corresponding to the interrupt request (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44),

[†] chipset - a number of integrated circuits designed to perform one or more related functions, e.g., FIFO, registers, logic circuit in the interrupt control device for interrupt controlling function

- wherein the chipset (i.e., at said System control components) includes and an interrupt controller (i.e., interrupt control device 3 of Fig. 1) having a configuration circuit (i.e., logic circuit 4 and registers 6,7 in Fig. 1),
  - wherein the configuration circuit (i.e., said logic circuit and registers) is configured to store configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-52) indicating a location in a memory device (i.e., RAM 2 of Fig. 1) to store the interrupt information (See col. 4, lines 53-67);

- storing the interrupt information at a memory location (i.e., location at address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67) without notifying the first processor (i.e., said microprocessor) the interrupt request (See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller inherently anticipates storing the interrupt information at a memory location without notifying the processor the interrupt request); and
- polling the memory device (i.e., RAM 2 of Fig. 1) to check for the interrupt information (See col. 5, lines 61-63), wherein
  - polling is performed at a time independent from a time the interrupt request (i.e., event justifying an interruption) is received at the chipset (i.e., said System control components; See col. 2, lines 59-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said chipset (i.e., System control components), as disclosed by Athenes, in said chipset, as disclosed by Watson, for the advantage of avoiding a risk of

operation error that a subsequent interrupt signal (i.e., event) interrupts the processing of a preceding interrupt of the same type, issued by a same entity (See Athenes, col. 2, line 67 through col. 3, line 3).

Watson, as modified by Athenes, does not teach that the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle.

Moyer discloses an apparatus for reducing interrupt latency by dynamic buffer sizing (See Abstract), wherein

- a configuration circuit (i.e., Store Buffer of Fig. 1) is configured to store configuration data (i.e., limit control register 141 storing limit value of ADA slots in Fig. 2) indicating a number of devices (i.e., a number of ADA slots in Fig. 2) an interrupt controller (i.e., Control Logic 142 of Fig. 2) is configured to handle (See col. 4, lines 4+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., Store Buffer), as disclosed by Moyer, in said interrupt controller (i.e., interrupt control device), as disclosed by Watson, as modified by Athenes, for the advantage of providing the ability to decouple writes to long latency memory with reducing interrupt latency by dynamic buffer sizing (See Moyer, col. 1, lines 21-28 and col. 3, lines 6-32).

Referring to claim 22, Athenes teaches

- polling is performed by the first processor (i.e., microprocessor 1 of Fig. 1; See col. 5, lines 61-63).

Referring to claim 25, Watson, as modified by Athenes, teaches

- storing the interrupt information at the memory location (i.e., location at address of Word for interrupt in RAM 2 in Fig. 1; See Athenes, col. 3, lines 30-35 and col. 4, lines 45-67) includes storing the interrupt information (i.e., the origin of interrupt and reason for the interruption event; Athenes) in a memory device (i.e., Athenes's RAM 2 of Fig. 1, which is mapped to Watson's System Memory 130 of Fig. 2) separate from the first processor (i.e., one of the one or more processors 110 in Fig. 2; Watson), a second processor (i.e., the other one of the one or more processors 110 in Fig. 2; Watson) and the chipset (i.e., System control components in Fig. 1; See col. 3, lines 9-15; i.e., wherein in fact that RAM is common to microprocessor and to the different elements of the system, and is connected to the logic circuit of interrupt control device inherently anticipates a memory device separate from the processor and the chipset).

Referring to claim 26, Athenes teaches

- storing the interrupt information at the memory location (i.e., location at address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67) includes storing the interrupt information (i.e., the origin of interrupt and reason for the interruption event) at the memory location according to a configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67).

Referring to claim 27, Athenes teaches

- the configuration information (i.e., address of Word for interrupt in RAM 2 in Fig. 1) is stored in a random access memory device of the chipset (i.e., said address is stored in registers 6,7 of said System control components, actually, interrupt control device 3 in Fig. 1).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson [US 6,466,226 B1] in view of Athenes [US 6,192,441 B1] and Moyer [US 6,976,110 B2] as applied to claims 6-8, 10, 11, 21, 22, and 25-27 above, and further in view of Tseng [US 6,816,918 B2].

Referring to claim 9, Watson, as modified by Athenes and Moyer, discloses all the limitations of the claim 9, including the interrupt controller (i.e., interrupt control device 3 of Fig. 1; Athenes) having a logic circuit (i.e., logic circuit 4 of Fig. 1; Athenes) to receive the interrupt information (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-29), except that does not expressly teach a configuration circuit having a read only memory device to store the configuration address and configuration data.

Tseng discloses a flexible apparatus for setting configurations using an EEPROM (See Abstract), wherein

- a configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM in Fig. 3) having a read only memory device (i.e., said EEPROM in Fig. 3) to store configuration address and configuration data (i.e., storing address index and its contents; See col. 3, lines 35-39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM), as disclosed by Tseng, in said configuration circuit (i.e., logic circuit and registers), as disclosed by Watson, as modified by Athenes and Moyer, for the advantage of providing a method for flexibly configuring default location in the memory device (i.e., default value) of the integrated circuit (i.e., network device) through the read only memory (i.e., EEPROM interface; See Tseng, col. 2, lines 28-30).

9. Claims 12, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson [US 6,466,226 B1] in view of Athenes [US 6,192,441 B1] and Moyer [US 6,976,110 B2] as applied to claims 6-8, 10, 11, 21, 22, and 25-27 above, and further in view of Callway et al. [US 6,279,067 B1; hereinafter Callway].

Referring to claim 12, Watson, as modified by Athenes and Moyer, discloses all the limitations of the claim 12, including the processor (i.e., said one of the one or more processors 110 in Fig. 2 in Watson, which is mapped to microprocessor 1 of Fig. 1 in Athenes) configured to poll the memory device (i.e., RAM 2 of Fig. 1; Athenes) to check for the interrupt information (See Athenes, col. 5, lines 61-65) at a time independent from a time the interrupt information is received by the chipset (See Athenes, col. 2, lines 59-67), except that does not teach that the second processor is configured to perform said polling.

Callway discloses an apparatus for detecting interrupt requests in video graphics and other system (See Abstract), wherein

- a processor (i.e., video graphics processing block 16 of Fig. 2);
- a second processor (i.e., polling block 12 of Fig. 2) is configured to poll a memory device (i.e.,. registers 34, 44 in Fig. 2) to check for an interrupt information (i.e., IRQ flags; See col. 3, lines 22-28 and 51-57) at a time independent from a time the interrupt information is received by the chipset (i.e., VIP slaves 30, 40 in Fig. 2; See col. 3, lines 57-64, i.e., wherein in fact that polling block generates the required signals to access the registers of the VIP slaves, then determines that an interrupt request is pending implies that a second processor is configured to poll a memory device to check for an interrupt information at a time independent from a time the interrupt information is received by the chipset).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have configured said second processor (i.e., the other one of the one or more processors), as disclosed by Watson, as modified by Athenes and Moyer, to perform said polling, as disclosed by Callway, for the advantage of the performance of said processor (i.e., video graphics processing block) is not degraded by having to perform said polling functions by implementing said second processor (i.e., polling block) as separate circuitry from said processor (i.e., video graphics processing block; See Callway, col. 3, line 66 through col. 4, line 8).

Referring to claim 23, Watson, as modified by Athenes and Moyer, discloses all the limitations of the claim 23, including that the polling is performed by the first processor (i.e., microprocessor 1 of Fig. 1; See Athenes, col. 5, lines 61-63), except that does not teach that the polling is performed by a second processor.

Callway discloses a method for detecting interrupt requests in video graphics and other system (See Abstract), wherein

- a first processor (i.e., video graphics processing block 16 of Fig. 2);
- a second processor (i.e., polling block 12 of Fig. 2); wherein
    - polling is performed by the second processor (See col. 3, lines 57-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have configured said second processor (i.e., the other one of the one or more processors), as disclosed by Watson, as modified by Athenes and Moyer, to perform said polling, as disclosed by Callway, for the advantage of the performance of the first processor (i.e., video graphics processing block) is not degraded by having to perform the polling functions by implementing the second processor (i.e., polling block) as separate circuitry from the first

processor (i.e., video graphics processing block; See Callway, col. 3, line 66 through col. 4, line 8).

Referring to claim 24, Athenes teaches

- performing an interrupt function (i.e., interrupt processing) based on the interrupt information (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22) stored in the memory location (See col. 5, line 61 through col. 6, line 11). wherein
    - performing the interrupt function (i.e., said interrupt processing) is carried out by the first processor (See col. 5, lines 53-60).

10. Claims 13, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athenes [US 6,192,441 B1] in view of Moyer [US 6,976,110 B2].

Referring to claim 13, Athenes discloses a method (i.e., method of postponing processing of interrupts by a microprocessor; See Abstract) comprising:

- receiving an interrupt request (i.e., event justifying an interruption) at an interrupt controller (i.e., interrupt control device 3 of Fig. 1; See col. 3, lines 19-22);
- acquiring, at the interrupt controller (i.e., at said interrupt control device), interrupt information corresponding to the interrupt request (i.e., the origin of interrupt and reason for the interruption event; See col. 3, lines 19-22 and col. 4, lines 38-44),
    - wherein an interrupt controller (i.e., interrupt control device 3 of Fig. 1) includes a configuration circuit (i.e., logic circuit 4 and registers 6,7 in Fig. 1),
        - wherein the configuration circuit (i.e., said logic circuit and registers) is configured to store configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-

52) indicating a location in a memory device (i.e., RAM 2 of Fig. 1) to store the interrupt information (See col. 4, lines 53-67); and

- passing the interrupt information from the interrupt controller (i.e., said interrupt control device) to a memory device (i.e., RAM 2 of Fig. 1) without passing the interrupt information to a first processor (i.e., microprocessor 1 of Fig. 1; See col. 2, lines 59-67 and col. 3, lines 27-29; i.e., wherein in fact that an event which appears in a given entity U will not interrupt the processing of the preceding event, and further said logic circuit behaves as a DMA controller inherently anticipates passing the interrupt information from the interrupt controller to a memory device without passing the interrupt information to a first processor).

Athenes does not teach that the configuration circuit is further configured to store configuration data indicating a number of devices the interrupt controller is configured to handle.

Moyer discloses an apparatus for reducing interrupt latency by dynamic buffer sizing (See Abstract), wherein

- a configuration circuit (i.e., Store Buffer of Fig. 1) is configured to store configuration data (i.e., limit control register 141 storing limit value of ADA slots in Fig. 2) indicating a number of devices (i.e., a number of ADA slots in Fig. 2) an interrupt controller (i.e., Control Logic 142 of Fig. 2) is configured to handle (See col. 4, lines 4+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., Store Buffer), as disclosed by Moyer, in said interrupt controller (i.e., interrupt control device), as disclosed by Athenes, for the advantage of providing the ability to decouple writes to long latency memory with reducing interrupt latency by dynamic buffer sizing (See Moyer, col. 1, lines 21-28 and col. 3, lines 6-32).

Referring to claim 18, Athenes teaches

- the memory device (i.e., RAM 2 of Fig. 1) and the interrupt controller (i.e., interrupt control device 3 of Fig. 1) are located in separate chips (See col. 3, lines 9-15; i.e., wherein in fact that RAM is common to the different elements of the system, and is connected to the logic circuit of interrupt control device inherently anticipates that the memory device and the interrupt controller are located in separate chips, e.g., RAM memory chip and logic circuit chip).

Referring to claim 19, Athenes teaches

- passing the interrupt information (i.e., the origin of interrupt and reason for the interruption event) from the interrupt controller (i.e., interrupt control device 3 of Fig. 1) to the memory device (i.e., RAM 2 of Fig. 1; See col. 3, lines 19-25) includes writing the interrupt information to the memory device at a memory location according to the configuration address (i.e., address of Word for interrupt in RAM 2 in Fig. 1; See col. 3, lines 30-35 and col. 4, lines 45-67).

11. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Athenes [US 6,192,441 B1] in view of Moyer [US 6,976,110 B2] as applied to claims 13, 18, and 19 above, and further in view of Callway [US 6,279,067 B1].

Referring to claim 14, Athenes, as modified by Moyer, discloses all the limitations of the claim 14, including polling the memory device (i.e., RAM 2 of Fig. 1; Athenes) to check for the interrupt information (See Athenes, col. 5, lines 61-63), wherein polling is performed by the first processor (i.e., microprocessor 1 of Fig. 1; See Athenes, col. 5, lines 61-63), except that does not teach that the polling is performed by a second processor.

Callway discloses a method for detecting interrupt requests in video graphics and other system (See Abstract), wherein

- a first processor (i.e., video graphics processing block 16 of Fig. 2);
- a second processor (i.e., polling block 12 of Fig. 2); wherein,
    - polling is performed by the second processor (See col. 3, lines 57-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have configured said second processor (i.e., the other one of the one or more processors), as disclosed by Athenes, as modified by Moyer, for performing said polling, as disclosed by Callway, for the advantage of the performance of the first processor (i.e., video graphics processing block) is not degraded by having to perform the polling functions by implementing the second processor (i.e., polling block) as separate circuitry from the first processor (i.e., video graphics processing block; See Callway, col. 3, line 66 through col. 4, line 8).

Referring to claim 15, Athenes, as modified by Moyer and Callway, teaches

- polling is performed by the second processor (See Callway, col. 3, lines 57-64) at a time independent from a time the interrupt request (i.e., event justifying an interruption; Athenes) is received by the interrupt controller (i.e., interrupt control device 3 of Fig. 1; See Athenes, col. 2, lines 59-67).

Referring to claim 16, Athenes teaches

- performing an interrupt function (i.e., interrupt processing) based on the interrupt information (See col. 5, line 61 through col. 6, line 11), wherein

- performing the interrupt function (i.e., said interrupt processing) is carried out by the first processor (See col. 5, lines 53-60).

Referring to claim 17, Callway teaches

- the first processor (i.e., video graphics processing block 16 of Fig. 2) and the second processor (i.e., polling block 12 of Fig. 2) are connected to the interrupt controller (i.e., VIP Host 10 of Fig. 2) through a single processor interface (i.e., Register 14 of Fig. 2).

12. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Athenes [US 6,192,441 B1] in view of Moyer [US 6,976,110 B2] as applied to claims 13, 18, and 19 above, and further in view of Tseng [US 6,816,918 B2].

Referring to claim 20, Athenes, as modified by Moyer, discloses all the limitations of the claim 20, including the configuration address is stored in a memory device of the interrupt controller (See Athenes, col. 3, lines 30-35 and col. 4, lines 45-67), except that does not teach said memory device is a read only memory device.

Tseng discloses a flexible apparatus for setting configurations using an EEPROM (See Abstract), wherein

- a configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM in Fig. 3) including a read only memory device (i.e., said EEPROM in Fig. 3) to store configuration address (i.e., storing address index and its contents; See col. 3, lines 35-39).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said configuration circuit (i.e., configuration instruction interpreter, register file with downloadable register, and EEPROM), as disclosed by Tseng, in said interrupt

controller (i.e., interrupt control device), as disclosed by Athenes, as modified by Moyer, for the advantage of providing a method for flexibly configuring default location in the memory device (i.e., default value) of the integrated circuit (i.e., network device) through the read only memory (i.e., EEPROM interface; See Tseng, col. 2, lines 28-30).

Response to Arguments

13. Applicants' arguments filed on 24th of April 2006 have been fully considered but they are not persuasive.

In response to the Applicants' argument with respect to "Further, the Office Action refers to a system taught by Callway for an example of a second processor that performs the polling. However, Callway appears to teach a different system. ... Applicant requests documents or an affidavit to support the rejection of claim 12. ..." in the Response page 12, lines 1-8, the Examiner believes the Applicants misunderstand the claim 12 rejection.

At first, it has been held that a prior art reference must either be in the field of Applicants' endeavor or, if not, then be reasonably pertinent to the particular problem with which the Applicants were concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Callway reference is disclosing a method and apparatus for detecting an interrupt requests (See Abstract), which is reasonably pertinent to the particular problem with which the Applicants were concerned.

At second, in contrary to the Applicants' assertion, the Examiner had provided the document "Callway US patent" to support the rejection of claim 12 under the Official Notice (See page 12, lines 17-19 of the Non-Final Office Action mailed on 24th of January 2006).

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Claims 17 and 23 were rejected under 35 USC j 103(a) as being unpatentable over Athenes as applied to claim 13-16, 18-22, and 24-27 above, and further in view of Callway. ... because Applicant cannot find a motivation to combine Athens and Callway as proposed by the Office Action. ..." in the Response page 12, lines 9-23, the Examiner respectfully disagrees.

In contrary to the Applicants' statement, all the rejections under *35 USC §103(a)* in the prior and the instant Office Action established a *prima facie* case of obviousness meeting the three basic criteria of the MPEP 2143.03 (8th ed. 2001). See the Office Action mailed on on 24th of January 2006.

Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner has clearly pointed out rationale for appropriate combination of the references.

Thus, the Applicants' argument on this point is not persuasive.

14. Applicants' arguments with respect to claims 1-16, 18-22, 24-27 on pages 8-11, have been considered but are moot in view of the new grounds of rejection.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Short et al. [US 5,708,814 A] disclose method and apparatus for reducing the rate of interrupts by generating a single interrupt for a group of events.

Baxter et al. [US 6,477,600 B1] disclose apparatus and method for processing isochronous interrupts.

16. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant's are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Patent Examiner
Art Unit 2112

CEL/